ELPIDA

PRELIMINARY DATA SHEET

1G bits DDR3L SDRAM

EDJ1108EJBG (128M words × 8 bits)
EDJ1116EJBG (64M words × 16 bits)

Specifications

- Density: 1G bits
- Organization
— 16M words × 8 bits × 8 banks (EDJ1108EJBG)
— 8M words × 16 bits × 8 banks (EDJ1116EJBG)
- Package
— 78-ball FBGA (EDJ1108EJBG)
— 96-ball FBGA (EDJ1116EJBG)
— Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.35V (typ)
— VDD = 1.283V to 1.45V
— Backward compatible for VDD, VDDQ = 1.5V ± 0.075V
- Data rate
— 1866Mbps/1600Mbps/1333Mbps (max)
- 1KB page size (EDJ1108EJBG)
— Row address: A0 to A13
— Column address: A0 to A9
- 2KB page size (EDJ1116EJBG)
— Row address: A0 to A12
— Column address: A0 to A9
- Eight internal banks for concurrent operation
- Burst length (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
— Sequential (8, 4 with BC)
— Interleave (8, 4 with BC)
- /CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11, 13
- /CAS Write Latency (CWL): 5, 6, 7, 8, 9
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles
— Average refresh period
  7.8μs at 0°C ≤ TC ≤ +85°C
  3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
— TC = 0°C to +95°C

Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
— Synchronous ODT
— Dynamic ODT
— Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- /RESET pin for Power-up sequence and reset function
- SRT range:
— Normal/extended
- Programmable Output driver impedance control
- Seamless BL4 access with bank-grouping
— Applied only for DDR3-1333 and 1600

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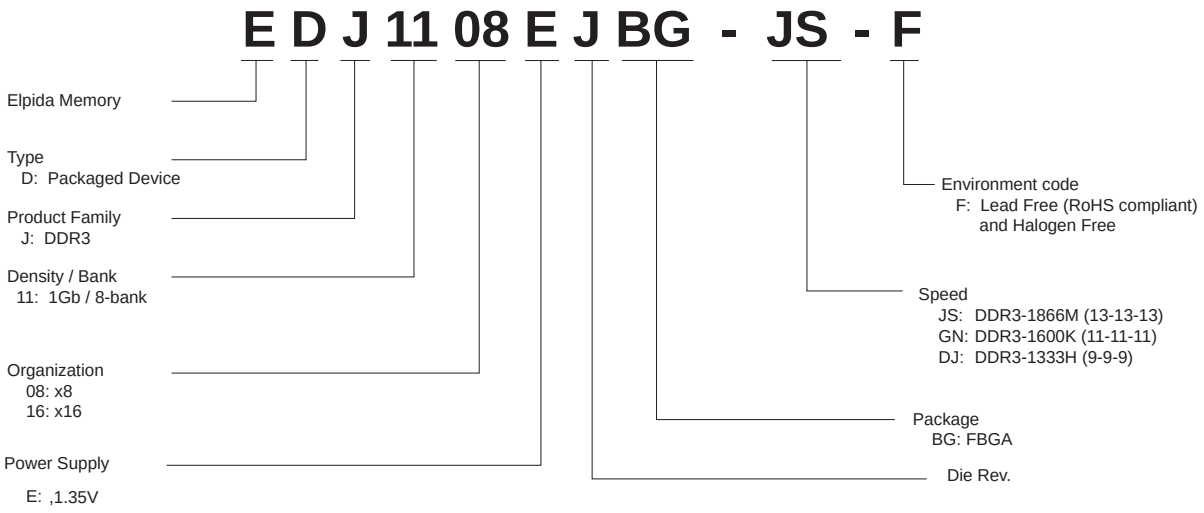
Ordering Information

Part number	Die revision	Organization (words × bits)	Internal banks	JEDEC speed bin (CL-tRCD-tRP)	Package
EDJ1108EJBG-JS-F	J	128M × 8	8	DDR3L-1866M (13-13-13)	78-ball FBGA
EDJ1108EJBG-GN-F				DDR3L-1600K (11-11-11)	
EDJ1108EJBG-DJ-F				DDR3L-1333H (9-9-9)	
EDJ1116EJBG-JS-F	J	64M × 16	8	DDR3L-1866M (13-13-13)	96-ball FBGA
EDJ1116EJBG-GN-F				DDR3L-1600K (11-11-11)	
EDJ1116EJBG-DJ-F				DDR3L-1333H (9-9-9)	

Note: 1. Please refer to the EDJ1108DJBG, EDJ1116DJBG datasheet (E1729E) when using this device at 1.5V operation, unless stated otherwise.

Part Number



Operating Frequency

Speed Grade	Frequency (Mbps) CL5	CL6	CL7	CL8	CL9	CL10	CL11	CL13	speed bin (CL-tRCD-tRP)
-JS	667	800	1066	1066	1333	1333	1600	1866	DDR3L-1866 (13-13-13)
-GN	667	800	1066	1066	1333	1333	1600		DDR3L-1600 (11-11-11)
-DJ	667	800	1066	1066	1333	1333			DDR3L-1333 (9-9-9)

Detailed Information

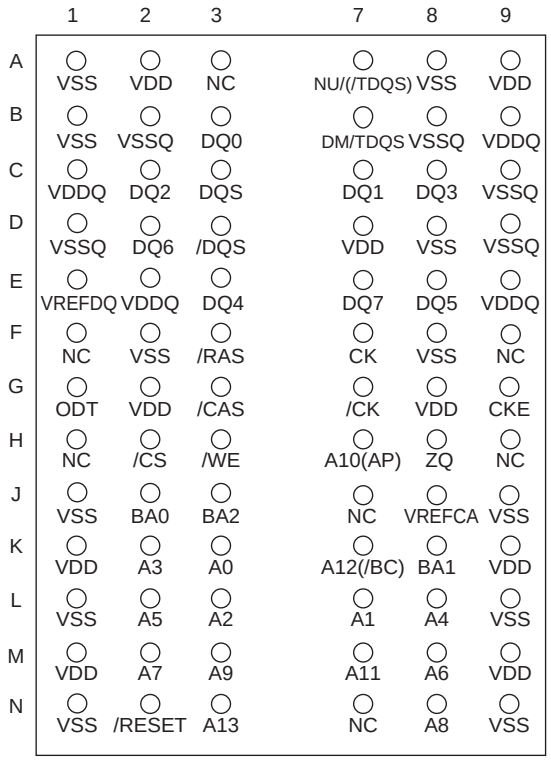
For detailed electrical specification and further information, please refer to the DDR3L SDRAM General Functionality and Electrical Condition data sheet (E1927E) and Addendum data sheet (E1928E).

Pin Configurations

Pin Configurations (×8 configuration)

/xxx indicates active low signal.

78-ball FBGA


1 2 3 7 8 9
A VSS VDD NC NU/(/TDQS) VSS VDD
B VSS VSSQ DQ0 DM/TDQS VSSQ VDDQ
C VDDQ DQ2 DQS DQ1 DQ3 VSSQ
D VSSQ DQ6 /DQS VDD VSS VSSQ
E VREFDQ VDDQ DQ4 DQ7 DQ5 VDDQ
F NC VSS /RAS CK VSS NC
G ODT VDD /CAS /CK VDD CKE
H NC /CS /WE A10(AP) ZQ NC
J VSS BA0 BA2 NC VREFCA VSS
K VDD A3 A0 A12(/BC) BA1 VDD
L VSS A5 A2 A1 A4 VSS
M VDD A7 A9 A11 A6 VDD
N VSS /RESET A13 NC A8 VSS

(Top view)

Pin name	Function	Pin name	Function
A0 to A13*3	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET*3	Active low asynchronous reset
BA0 to BA2*3	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
TDQS, /TDQS	Termination data strobe	VSSQ	Ground for DQ circuit
/CS*3	Chip select	VREFDQ	Reference voltage for DQ
/RAS, /CAS, /WE*3	Command input	VREFCA	Reference voltage for CA
CKE*3	Clock enable	ZQ	Reference pin for ZQ calibration
CK, /CK	Differential clock input	NC*1	No connection
DM	Write data mask	NU*2	Not usable
ODT*3	ODT control		

Notes: 1. Not internally connected with die.
2. Don't connect. Internally connected.
3. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

Pin Configurations (× 16 configuration)

/xxx indicates active low signal.

96-ball FBGA

	1	2	3	7	8	9
A	VDDQ	DQU5	DQU7	DQU4	VDDQ	VSS
B	VSSQ	VDD	VSS	/DQSU	DQU6	VSSQ
C	VDDQ	DQU3	DQU1	DQSU	DQU2	VDDQ
D	VSSQ	VDDQ	DMU	DQU0	VSSQ	VDD
E	VSS	VSSQ	DQL0	DML	VSSQ	VDDQ
F	VDDQ	DQL2	DQSL	DQL1	DQL3	VSSQ
G	VSSQ	DQL6	/DQSL	VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQL4	DQL7	DQL5	VDDQ
J	NC	VSS	/RAS	CK	VSS	NC
K	ODT	VDD	/CAS	/CK	VDD	CKE
L	NC	/CS	/WE	A10(AP)	ZQ	NC
M	VSS	BA0	BA2	NC	VREFCA	VSS
N	VDD	A3	A0	A12(/BC)	BA1	VDD
P	VSS	A5	A2	A1	A4	VSS
R	VDD	A7	A9	A11	A6	VDD
T	VSS	/RESET	NC	NC	A8	VSS

(Top view)

Pin name	Function	Pin name	Function
A0 to A12*2	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET*2	Active low asynchronous reset
BA0 to BA2*2	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	Data input/output	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS*2	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE*2	Command input	VREFDQ	Reference voltage for DQ
CKE*2	Clock enable	VREFCA	Reference voltage for CA
CK, /CK	Differential clock input	ZQ	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC*1	No connection
ODT*2	ODT control		

Notes: 1. Not internally connected with die.

2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

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1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	–0.4 to +1.975	V	1, 3
Power supply voltage for output	VDDQ	–0.4 to +1.975	V	1, 3
Input voltage	VIN	–0.4 to +1.975	V	1
Output voltage	VOUT	–0.4 to +1.975	V	1
Reference voltage	VREFCA	–0.4 to 0.6 × VDD	V	3
Reference voltage for DQ	VREFDQ	–0.4 to 0.6 × VDDQ	V	3
Storage temperature	Tstg	–55 to +100	°C	1, 2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.

3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)

   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

1.3 Recommended DC Operating Conditions

Table 3: Recommended DC Operating Conditions (TC = 0°C to +85°C), DDR3L Operation

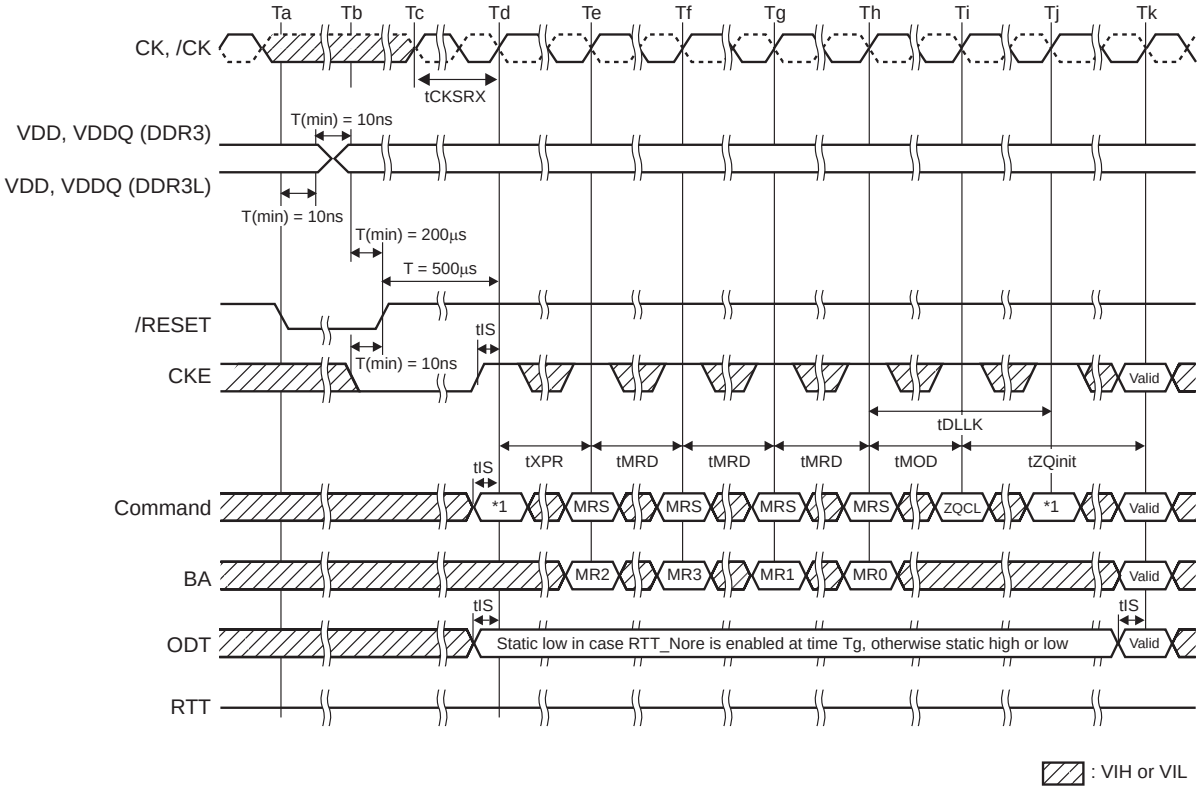
Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD	1.283	1.35	1.45	V	1, 2, 3, 4
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1, 2, 3, 4

Notes: 1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g. 1 sec).
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specifcation.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while
5. VDD and VDDQ are changed for DDR3 operation shown as following timing wave form.

Table 4: Recommended DC Operating Conditions (TC = 0°C to +85°C), DDR3 Operation

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2, 3

Notes: 1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifcations under the same speedtimings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation shown as below.



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 1: VDD/VDDQ Voltage Switch between DDR3L and DDR3

1.4 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

  Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC)max
- H and 1: VIN ≥ VIH(AC)min
- MID-LEVEL: defined as inputs are VREF = VDDQ / 2
- FLOATING: don't care or floating around VREF.
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.

  Note:The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting.

  RON = RZQ/7 (34Ω in MR1);

  Qoff = 0B (Output Buffer enabled in MR1);

  RTT_Nom = RZQ/6 (40Ω in MR1);

  RTT_WR = RZQ/2 (120Ω in MR2);

  TDQS Feature disabled in MR1
- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} : = {H, H, H, H}

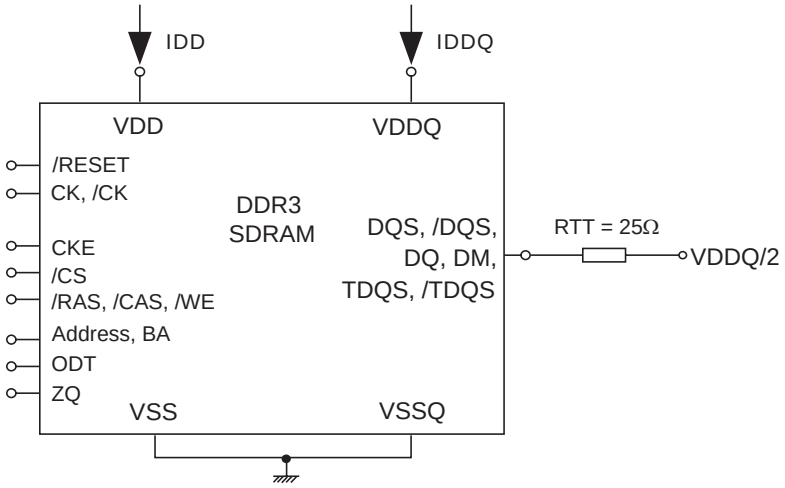


Figure 2: Measurement Setup and Test Load for IDD and IDDQ Measurements

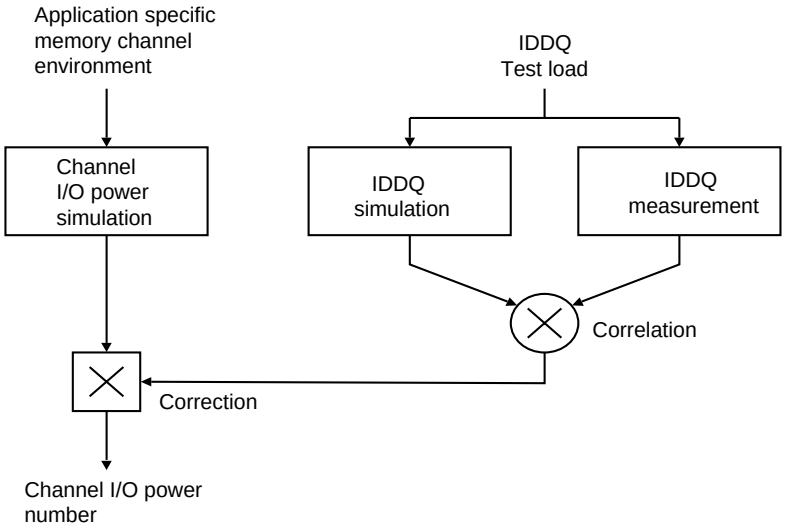


Figure 3: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

1.4.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 5: Timings Used for IDD and IDDQ Measurement-Loop Patterns

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	
Parameter	**6-6-6**	**7-7-7**	**9-9-9**	**11-11-11**	**Unit**
CL	6	7	9	11	nCK
tCK(min)	2.5	1.875	1.5	1.25	ns
nRCD(min)	6	7	9	11	nCK
nRC(min)	21	27	33	39	nCK
nRAS(min)	15	20	24	28	nCK
nRP(min)	6	7	9	11	nCK
nFAW (1KB)	16	20	20	24	nCK
nFAW (2KB, 4KB)	20	27	30	32	nCK
nRRD (1KB)	4	4	4	5	nCK
nRRD (2KB, 4KB)	4	6	5	6	nCK
nRFC (1Gb)	44	59	74	88	nCK
nRFC (2Gb)	64	86	107	128	nCK
nRFC (4Gb)	104	139	174	208	nCK

	DDR3-1866	
Parameter	**13-13-13**	**Unit**
CL	13	nCK
tCK(min)	1.07	ns
nRCD(min)	13	nCK
nRC(min)	45	nCK
nRAS(min)	32	nCK
nRP(min)	13	nCK
nFAW (1KB)	26	nCK
nFAW (2KB, 4KB)	33	nCK
nRRD (1KB)	5	nCK
nRRD (2KB, 4KB)	6	nCK
nRFC (1Gb)	103	nCK
nRFC (2Gb)	150	nCK
nRFC (4Gb)	243	nCK

1.4.2 Basic IDD and IDDQ Measurement Conditions

Table 6: Basic IDD and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 5; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 7; Data I/O: MID-LEVEL; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 7); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 7
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 5; BL: 8*1, *6; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 8; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 8); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 8
Precharge standby current	IDD2N	CKE: H; External clock: on; tCK, CL: see Table 5 BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 9; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see Table 9
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 10; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 10; pattern details: see Table 10
Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge power-down current slow exit	IDD2P0	CKE: L; External clock: on; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 9; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 9
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 5; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to Table 11; data I/O: seamless read data burst with different data between one burst and the next one according to Table 11; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 11); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 11
Operating burst read IDDQ current	IDDQ4R	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

Table 6: Basic IDD and IDDQ Measurement Conditions (cont'd)

Parameter	Symbol	Description
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 5; BL: 8*1; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to Table 12; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,.. (see Table 12); Output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 12
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 5; BL: 8*1; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to Table 13; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC (Table 13); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 13
Self-refresh current: normal temperature range	IDD6	TC: 0 to 85°C; ASR: disabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: see Table 5; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self-refresh current: extended temperature range	IDD6ET	TC: 0 to 95°C; ASR: Disabled*4; SRT: Extended*5; CKE: L; External clock: off; CK and /CK: L; CL: Table 5; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Auto self-refresh current (Optional)	IDD6TC	TC: 0 to 95°C; ASR: Enabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: Table 5; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Auto self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 5; BL: 8*1, *6; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to Table 14; data I/O: read data bursts with different data between one burst and the next one according to Table 14; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Table 14; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 14
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
2. MR: Mode Register
Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];
RTT_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT_WR enable: set MR2 bits [10, 9] = [1,0].
3. Precharge power down mode: set MR0 bit A12= 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.
4. Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.
5. Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.
6. Read burst type: nibble sequential, set MR0 bit A3 = 0

Table 7: IDD0 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	
			…	Repeat pattern 1…4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	
			…	Repeat pattern 1...4 until nRC – 1, truncate if necessary												
			1 × nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	
			1 × nRC +1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	
			1 × nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
			…	Repeat pattern nRC + 1,...,4 until 1 × nRC + nRAS – 1, truncate if necessary												
			1 × nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	
			…	Repeat nRC + 1,...,4 until 2 × nRC – 1, truncate if necessary												
		1	2 × nRC	Repeat Sub-Loop 0, use BA= 1 instead												
		2	4 × nRC	Repeat Sub-Loop 0, use BA= 2 instead												
		3	6 × nRC	Repeat Sub-Loop 0, use BA= 3 instead												
		4	8 × nRC	Repeat Sub-Loop 0, use BA= 4 instead												
		5	10 × nRC	Repeat Sub-Loop 0, use BA= 5 instead												
		6	12 × nRC	Repeat Sub-Loop 0, use BA= 6 instead												
		7	14 × nRC	Repeat Sub-Loop 0, use BA= 7 instead												

Notes: 1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 8: IDD1 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	—
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	—
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	—
			…	Repeat pattern 1...4 until nRCD – 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			…	Repeat pattern 1...4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	—
			…	Repeat pattern 1...4 until nRC – 1, truncate if necessary												
			1 × nRC + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	—
			1 × nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	—
			1 × nRC + 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	—
			…	Repeat pattern nRC + 1,..., 4 until nRC + nRCD – 1, truncate if necessary												
			1 × nRC + nRCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			…	Repeat pattern nRC + 1,..., 4 until nRC +nRAS – 1, truncate if necessary												
			1 × nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	—
			…	Repeat pattern nRC + 1,..., 4 until 2 × nRC – 1, truncate if necessary												
		1	2 × nRC	Repeat Sub-Loop 0, use BA= 1 instead												
		2	4 × nRC	Repeat Sub-Loop 0, use BA= 2 instead												
		3	6 × nRC	Repeat Sub-Loop 0, use BA= 3 instead												
		4	8 × nRC	Repeat Sub-Loop 0, use BA= 4 instead												
		5	10 × nRC	Repeat Sub-Loop 0, use BA= 5 instead												
		6	12 × nRC	Repeat Sub-Loop 0, use BA= 6 instead												
		7	14 × nRC	Repeat Sub-Loop 0, use BA= 7 instead												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 9: IDD2N and IDD3N Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	
			1	D	1	0	0	0	0	0	0	0	0	0	0	
			2	/D	1	1	1	1	0	0	0	0	0	F	0	
			3	/D	1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, use BA= 1 instead												
		2	8 to 11	Repeat Sub-Loop 0, use BA= 2 instead												
		3	12 to 15	Repeat Sub-Loop 0, use BA= 3 instead												
		4	16 to 19	Repeat Sub-Loop 0, use BA= 4 instead												
		5	20 to 23	Repeat Sub-Loop 0, use BA= 5 instead												
		6	24 to 27	Repeat Sub-Loop 0, use BA= 6 instead												
		7	28 to 31	Repeat Sub-Loop 0, use BA= 7 instead												

Notes: 1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 10: IDD2NT and IDDQ2NT Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	
			1	D	1	0	0	0	0	0	0	0	0	0	0	
			2	/D	1	1	1	1	0	0	0	0	0	F	0	
			3	/D	1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, but ODT = 0 and BA= 1												
		2	8 to 11	Repeat Sub-Loop 0, but ODT = 1 and BA= 2												
		3	12 to 15	Repeat Sub-Loop 0, but ODT = 1 and BA= 3												
		4	16 to 19	Repeat Sub-Loop 0, but ODT = 0 and BA= 4												
		5	20 to 23	Repeat Sub-Loop 0, but ODT = 0 and BA= 5												
		6	24 to 27	Repeat Sub-Loop 0, but ODT = 1 and BA= 6												
		7	28 to 31	Repeat Sub-Loop 0, but ODT = 1 and BA= 7												

Notes: 1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 11: IDD4R and IDDQ4R Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	—
			2,3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	—
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	—
			6,7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	—
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 12: IDD4W Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	—
			2,3	/D, /D	1	1	1	1	1	0	0	0	0	0	0	—
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	—
			6,7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	—
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to write commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ signal by write command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 13: IDD5B Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	—
			1, 2	D	1	0	0	0	0	0	0	0	0	0	0	—
			3,4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	—
		1	5 to 8	Repeat cycles 1...4, but BA= 1												
			9 to 12	Repeat cycles 1...4, but BA= 2												
			13 to 16	Repeat cycles 1...4, but BA= 3												
			17 to 20	Repeat cycles 1...4, but BA= 4												
			21 to 24	Repeat cycles 1...4, but BA= 5												
			25 to 28	Repeat cycles 1...4, but BA= 6												
			29 to 32	Repeat cycles 1...4, but BA= 7												
		2	33 to nRFC – 1	Repeat Sub-Loop 1, until nRFC – 1. Truncate, if necessary.												

Notes: 1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 14: IDD7 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	—
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	—
			…	Repeat above D Command until nRRD – 1												
		1	nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	—
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	—
			…	Repeat above D Command until 2 × nRRD – 1												
		2	2 × nRRD	Repeat Sub-Loop 0, but BA= 2												
		3	3 × nRRD	Repeat Sub-Loop 1, but BA= 3												
		4	4 × nRRD	D	1	0	0	0	0	3	0	0	0	F	0	—
				Assert and repeat above D Command until nFAW – 1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but BA= 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA= 5												
		7	nFAW + 2 × nRRD	Repeat Sub-Loop 0, but BA= 6												
		8	nFAW + 3 × nRRD	Repeat Sub-Loop 1, but BA= 7												
		9	nFAW	D	1	0	0	0	0	7	0	0	0	F	0	—
			+ 4 × nRRD	Assert and repeat above D Command until 2 × nFAW – 1, if necessary												
		10	2 × nFAW + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	—
			2 × nFAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 × nFAW	D	1	0	0	0	0	0	0	0	0	F	0	—
			+ 2	Repeat above D Command until 2 × nFAW + nRRD – 1												
		11	2 × nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	—
			2 × nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 × nFAW	D	1	0	0	0	0	1	0	0	0	0	0	—
			+ nRRD + 2	Repeat above D Command until 2 × nFAW + 2 × nRRD – 1												
		12	2 × nFAW +2 × nRRD	Repeat Sub-Loop 10, but BA= 2												
		13	2 × nFAW + 3 × nRRD	Repeat Sub-Loop 11, but BA= 3												
		14	2 × nFAW	D	1	0	0	0	0	3	0	0	0	0	0	—
			+ 4 × nRRD	Assert and repeat above D Command until 3 × nFAW – 1, if necessary												
		15	3 × nFAW	Repeat Sub-Loop 10, but BA= 4												
		16	3 × nFAW +nRRD	Repeat Sub-Loop 11, but BA= 5												
		17	3 × nFAW + 2 × nRRD	Repeat Sub-Loop 10, but BA= 6												
		18	3 × nFAW + 3 × nRRD	Repeat Sub-Loop 11, but BA= 7												
		19	3 × nFAW	D	1	0	0	0	0	7	0	0	0	0	0	—
			+ 4 × nRRD	Assert and repeat above D Command until 4 × nFAW – 1, if necessary												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

2. Electrical Specifications

2.1 DC Characteristics

Table 15: DC Characteristics 1 (TC = 0°C to +85°C, VDD, VDDQ = 1.283V to 1.45V)

		Data rate	× 8	× 16		
Parameter	**Symbol**	**(Mbps)**	**max**	**max**	**Unit**	**Notes**
Operating current (ACT-PRE)	IDD0	1333	48	55	mA	
		1600	52	60		
		1866	TBD	TBD		
Operating current (ACT-RD-PRE)	IDD1	1333	60	70	mA	
		1600	65	75		
		1866	TBD	TBD		
Precharge power-down standby current	IDD2P1	1333	20	20	mA	Fast PD Exit
		1600	20	20		
		1866	TBD	TBD		
	IDD2P0	1333	10	10	mA	Slow PD Exit
		1600	10	10		
		1866	TBD	TBD		
Precharge standby current	IDD2N	1333	30	30	mA	
		1600	30	30		
		1866	TBD	TBD		
Precharge standby ODT current	IDD2NT	1333	30	30	mA	
		1600	32	32		
		1866	TBD	TBD		
Precharge quiet standby current	IDD2Q	1333	30	30	mA	
		1600	30	30		
		1866	TBD	TBD		
Active power-down current (Always fast exit)	IDD3P	1333	25	25	mA	
		1600	25	26		
		1866	TBD	TBD		
Active standby current	IDD3N	1333	40	40	mA	
		1600	45	45		
		1866	TBD	TBD		
Operating current (Burst read operating)	IDD4R	1333	90	105	mA	
		1600	105	120		
		1866	TBD	TBD		
Operating current (Burst write operating)	IDD4W	1333	100	135	mA	
		1600	115	155		
		1866	TBD	TBD		
Burst refresh current	IDD5B	1333	135	135	mA	
		1600	140	140		
		1866	TBD	TBD		
All bank interleave read current	IDD7	1333	160	165	mA	
		1600	160	190		
		1866	TBD	TBD		
RESET low current	IDD8		10	10	mA	

Table 16: Self-Refresh Current (TC = 0°C to +85°C, VDD, VDDQ = 1.283V to 1.45V)

Parameter	Symbol	max	Unit	Notes
Self-refresh current normal temperature range	IDD6	10	mA	
Self-refresh current extended temperature range	IDD6ET	12	mA	
Auto self-refresh current (Optional)	IDD6TC	—	mA	

2.2 Pin Capacitance

Table 17: Pin Capacitance [DDR3-800 to 1600] (TC = 25°C, VDD, VDDQ = 1.283V to 1.45V)

		DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Input/output capacitance	CIO	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2	pF	1, 2
Input capacitance, CK and /CK	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	–0.5	0.3	–0.5	0.3	–0.4	0.2	–0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All addres/command input-only pins)	CDI_ADD_CMD	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	—	3	—	3	—	3	—	3	pF	2, 11

Table 18: Pin Capacitance [DDR3-1866 to 2133] (TC = 25°C, VDD, VDDQ = 1.283V to 1.45V)

		DDR3L-1866			
Parameter	Symbol	Min	Max	Units	Notes
Input/output capacitance	CIO	1.4	2.1	pF	1, 2
Input capacitance, CK and /CK	CCK	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.2	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	–0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All addres/command input-only pins)	CDI_ADD_CMD	–0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	–0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	—	3	pF	2, 11

Notes: 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.
2. VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.35V, VBIAS=VDD/2 and ondie termination off.

3. Absolute value of CCK-C/CK.
4. Absolute value of CIO(DQS)-CIO(/DQS).
5. CI applies to ODT, /CS, CKE, A0-A15, BA0-BA2, /RAS, /CAS and /WE.
6. CDI_CTRL applies to ODT, /CS and CKE.
7. CDI_CTRL = CI(CTRL) − 0.5 × (CI(CK)+CI(/CK)).
8. CDI_ADD_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.
9. CDI_ADD_CMD = CI(ADD_CMD) − 0.5 × (CI(CK)+CI(/CK)).
10. CDIO=CIO(DQ,DM) − 0.5 × (CIO(DQS)+CIO(/DQS)).
11. Maximum external load capacitance on ZQ pin: 5pF.

2.3 Standard Speed Bins

Table 19: DDR3-800 Speed Bins

Speed Bin		DDR3-800E			
CL-tRCD-tRP		6-6-6			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		15	20	ns	10
tRCD		15	—	ns	10
tRP		15	—	ns	10
tRC		52.5	—	ns	10
tRAS		37.5	9 × tREFI	ns	9
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 11
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 11
Supported CL settings			5, 6	nCK	
Supported CWL settings			5	nCK	

Table 20: DDR3-1066 Speed Bins

Speed Bin		DDR3-1066F			
CL-tRCD-tRP		7-7-7			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.125	20	ns	10
tRCD		13.125	—	ns	10
tRP		13.125	—	ns	10
tRC		50.625	—	ns	10
tRAS		37.5	9 × tREFI	ns	9
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 5, 11
	CWL = 6	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 5
	CWL = 6	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3
Supported CL settings			5, 6, 7, 8	nCK	
Supported CWL settings			5, 6	nCK	

Table 21: DDR3-1333 Speed Bins

Speed Bin		DDR3-1333H			
CL-tRCD-tRP		9-9-9			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.5 (13.125)	20	ns	10
tRCD		13.5 (13.125)	—	ns	10
tRP		13.5 (13.125)	—	ns	10
tRC		49.5 (49.125)	—	ns	10
tRAS		36	9 × tREFI	ns	9
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 6, 11
	CWL = 6, 7	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4, 6
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 6
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	ns	1, 2, 3, 4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	ns	1, 2, 3
Supported CL settings		5, 6, 7, 8, 9, 10		nCK	
Supported CWL settings		5, 6, 7		nCK	

Table 22: DDR3-1600 Speed Bins

Speed Bin		DDR3-1600K			
CL-tRCD-tRP		11-11-11			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.75 (13.125)	20	ns	10
tRCD		13.75 (13.125)	—	ns	10
tRP		13.75 (13.125)	—	ns	10
tRC		48.75 (48.125)	—	ns	10
tRAS		35	9 × tREFI	ns	9
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 7, 11
	CWL = 6, 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	ns	1, 2, 3, 4, 7
	CWL= 8	Reserved	Reserved	ns	4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	< 1.875	ns	1, 2, 3, 7
	CWL= 8	Reserved	Reserved	ns	4
tCK(avg) @CL=11	CWL = 5, 6, 7	Reserved	Reserved	ns	4
	CWL= 8	1.25	< 1.5	ns	1, 2, 3
Supported CL settings		5, 6, 7, 8, 9, 10, 11		nCK	
Supported CWL settings		5, 6, 7, 8		nCK	

Table 23: DDR3-1866 Speed Bins

Speed Bin		DDR3-1866M			
CL-tRCD-tRP		13-13-13			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.91	20.0	ns	
tRCD		13.91	—	ns	
tRP		13.91	—	ns	
tRC		47.91	—	ns	
tRAS		34.0	9 × tREFI	ns	9
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 8
	CWL = 6, 7, 8, 9	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 8
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7, 8, 9	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	2.5	ns	1, 2, 3, 8
	CWL = 7, 8, 9	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	2.5	ns	1, 2, 3, 8
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8, 9	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	1.875	ns	1, 2, 3, 8
	CWL= 8	Reserved	Reserved	ns	4
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	1.875	ns	1, 2, 3, 8
	CWL= 8	Reserved	Reserved	ns	4
tCK(avg) @CL=11	CWL = 5, 6, 7	Reserved	Reserved	ns	4
	CWL= 8	1.25	1.5	ns	1, 2, 3, 8
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=12	CWL = 5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=13	CWL = 5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL= 9	1.07	1.25	ns	4
Supported CL settings		5, 6, 7, 8, 9, 10, 11, 13		nCK	1, 2, 3, 8
Supported CWL settings		5, 6, 7, 8, 9		nCK	

Notes: 1. The CL setting and CWL setting result in tCK(avg)min and tCK(avg)max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

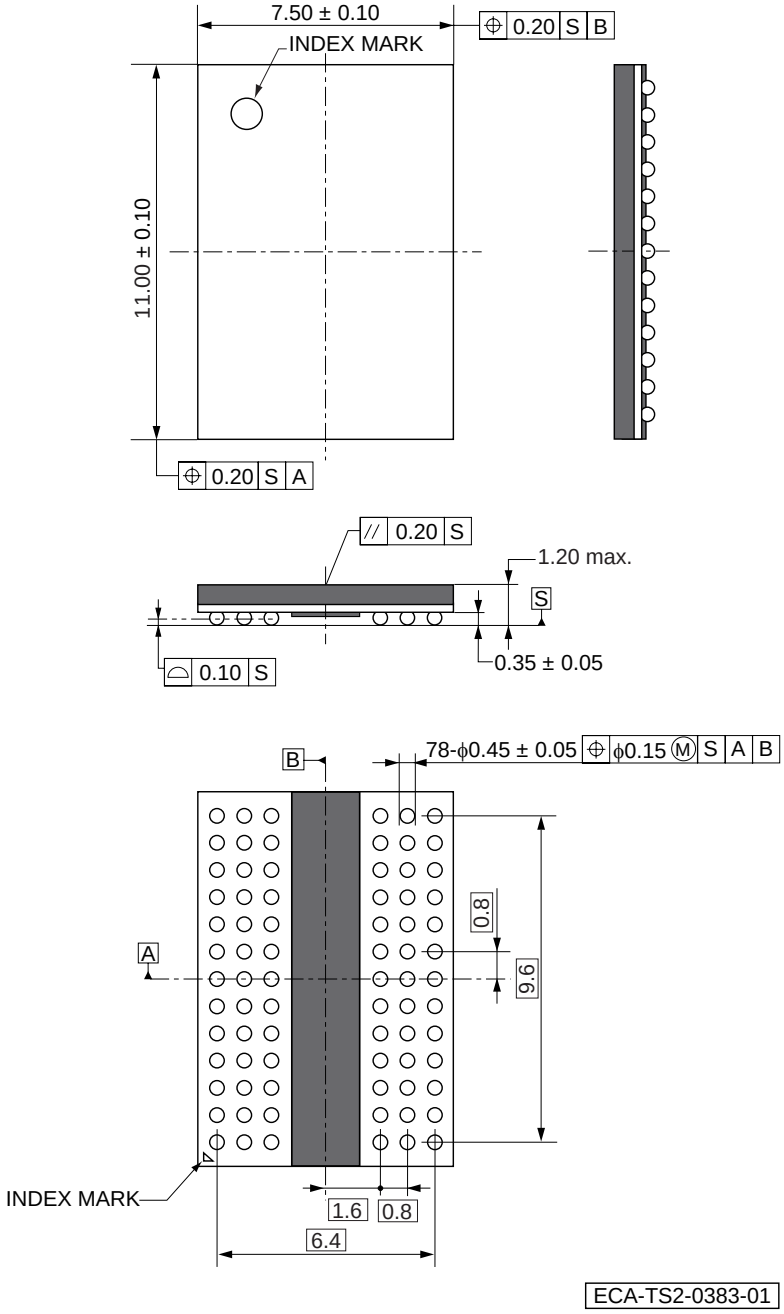
2. tCK(avg)min limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (3.0, 2.5, 1.875, 1.5, or 1.25ns) when calculating CL(nCK) = tAA(ns) / tCK(avg)(ns), rounding up to the next 'Supported CL'.
3. tCK(avg)max limits: Calculate tCK(avg) + tAA(max)/CL selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK(avg)max corresponding to CL selected.
4. Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1066 Speed Bins which are not subject to production tests but verified by design/characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1866 Speed Bins which is not subject to production tests but verified by design/characterization.
9. tREFI depends on operating case temperature (TC).
10. For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min) must be 13.125 ns or lower. SPD settings must be programmed to match.
11. DDR3-800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

3. Package Drawing

3.1 78-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

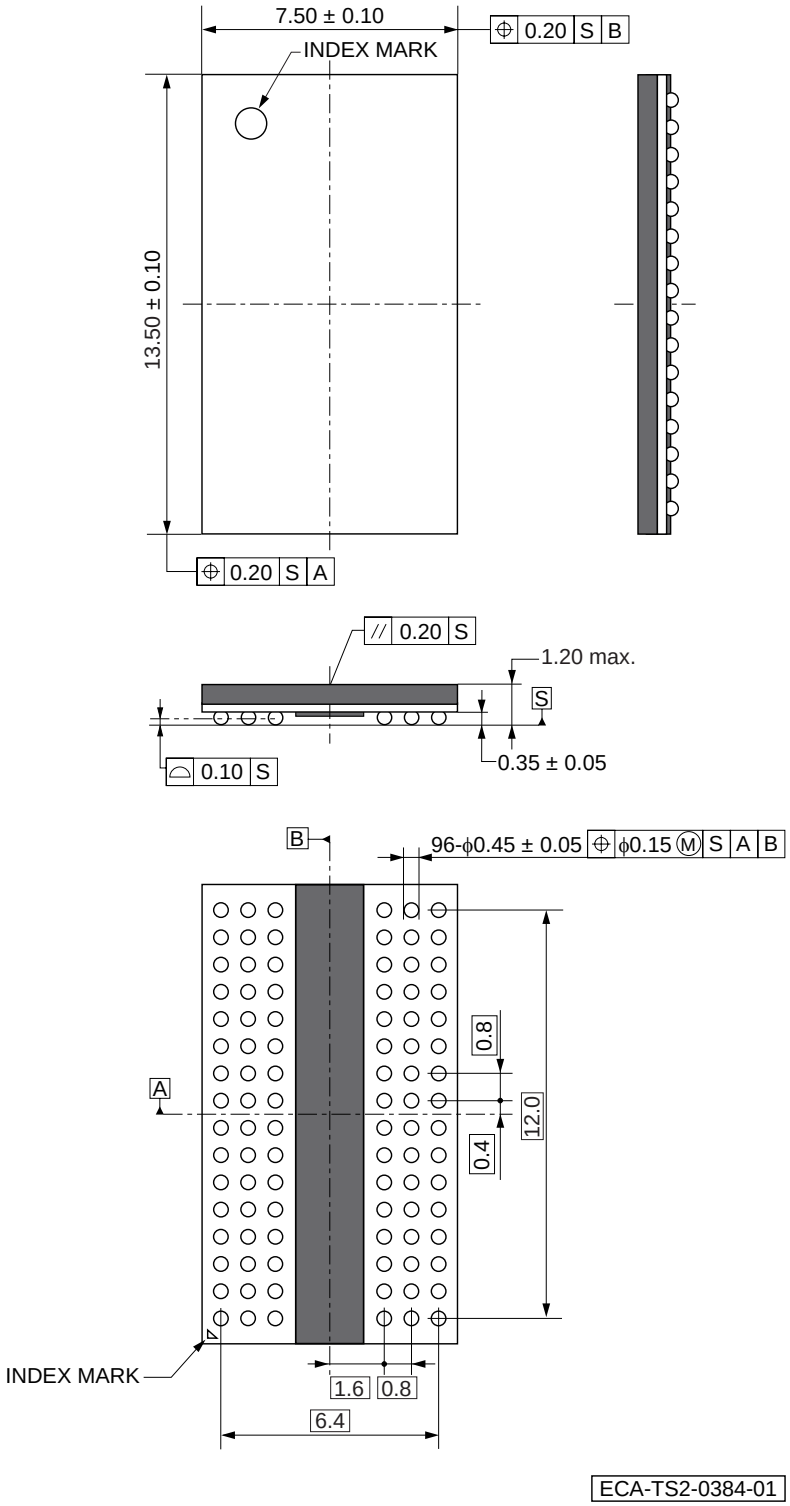
Unit: mm



3.2 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



ECA-TS2-0384-01

4. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the 1G bits DDR3 SDRAM.

Type of Surface Mount Device

EDJ1108EJBG: 78-ball FBGA < Lead free (Sn-Ag-Cu) >
EDJ1116EJBG: 96-ball FBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
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